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Jan Carol Little
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
WANG, TED M	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/039,248	MAURITZ ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7-14,16,17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5, 7-14, 16, 17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 1, 3, 5, 7-14, 16, 17 and 19 are withdrawn in view of the newly discovered reference(s) to US 6,996,632. Rejections based on the newly cited reference(s) follow.

2. Applicant's arguments, filed on 1/22/2007, with respect to the rejection(s) of claim 20 under 35 USC 102(b) has been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of US 6,996,632.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

- Claim 1, line 3, change "multiphase lock loop" to --- multiphase phase lock loop ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

((e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 3, 5, 7-14, 16, 17 and 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Levy et al. (US 6,996,632).

- With regard claim 1, Levy et al. discloses a system (Fig.2 element 200 and column 5 lines 31-41), comprising:

  a bus (Fig.2 element 206 and column 5 lines 2-58);

  first logic (Fig.5 element 500) having a multiphase lock loop to generate a multiphase encoded waveform (column 8 lines 25-30), the first logic including an input register (Fig.5 element 530 and column 8 lines 34-37) to receive at least one data word or at least one command/control word (Fig.5 element 530 input, D/C, and column 8 lines 32-33), and wherein the command/control word is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure (column 8 lines 34-37 and column 2 line 66 – column 3 line 3); and

  second logic (Fig.6 element 600) coupled to the first logic to drive the multiphase encoded waveform onto the bus (column 8 lines 38-43).

- With regard claim 3, Levy et al. further discloses wherein second logic includes third logic (Fig.6 elements 610 and 612) to generate differential signal levels representing the multiphase encoded waveform (column 8 lines 40-50).
- With regard claim 5, Levy et al. further discloses wherein the input register comprises a first-in-first-out (FIFO) register (Fig.5 element 530).
- With regard claim 7, Levy et al. further discloses wherein the bus includes at least one differential transmission line to receive signal levels for the multiphase encoded waveform (column 7 lines 11-21, where both driver (500 and 600) and receiver (400) are differential driver and receiver.)
- With regard claim 8, Levy et al. further discloses wherein second logic further comprises impedance matching circuitry to match impedance of the second logic to the differential transmission line (column 7 lines 17-21 and column 8 lines 41-44).
- With regard claim 9, Levy et al. further discloses a third logic coupled to the bus to receive the multiphase encoded waveform (Fig.2 element 204 and Fig.4 element 400 and column 7 lines 41-44 and 59-62).
- With regard claim 10, Levy et al. further discloses wherein the third logic includes an amplifier (Fig.4 element 402) to receive differential signal levels representing the multiphase encoded waveform from the bus and extract the multiphase encoded waveform from the received differential signal levels (column 7 lines 41-44).

- With regard claim 11, Levy et al. further discloses wherein the third logic includes a differential delayed lock loop (Fig.4 element 404) coupled to stretch a multiphase encoded waveform timing to a predetermined length (column 7 lines 44-51, where the third logic (Fig.4) of the Levys' reference is exactly the same (structure and connection and components) as that of the third logic (Fig.6) of the instant application, it is inherent that the differential DLL (404) of the Levys' third logic can perform the same function as that of the DLL (604) of the instant application, i.e. to stretch a multiphase encoded waveform timing to a predetermined length).
- With regard claim 12, Levy et al. further discloses wherein the third logic includes a register coupled to check data integrity of the multiphase encoded waveform (Fig.4 element DATA REGISTER AND INTEGRITY CHECK).
- With regard claim 13, Levy et al. discloses an apparatus, comprising:

  a device driver (Fig.5 element 500 and Fig.6 element 600 and column 8 lines 25 and 38-44) having first logic to generate a multiphase encoded waveform (Fig.5 element 500 and column 8 lines 25-30) and second logic coupled to the first logic to drive the multiphase encoded waveform onto a bus (Fig.6 element 600 and 8 lines 38-44),

  wherein second logic includes third logic to generate differential signal levels representing the multiphase encoded waveform (Fig.6 elements 610 and 612 and column 8 lines 44-50), and

wherein the first logic includes a command/control signal input (Fig.5 element 530 input, D/C, and column 8 lines 36-38),

wherein a command/control signal on the command/control signal input is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure (column 8 lines 34-37 and column 2 line 66 – column 3 line 3).

- With regard claim 14, Levy et al. further discloses wherein first logic (Fig.5 element 500) including a multiphase phase lock loop (Fig.5 elements 502-514) to generate a multiphase encoded waveform (column 8 lines 25-30).
- With regard claim 16, Levy et al. further discloses wherein the first logic includes an input register (Fig.5 element 530 and column 8 lines 34-37), coupled to the multiphase phase lock loop (Fig.5 elements 502-514), to receive at least one data word or at least one command/control word (Fig.5 element 530 input, D/C, and column 8 lines 32-33).
- With regard claim 17, Levy et al. further discloses wherein the input register comprises a first-in-first-out (FIFO) register (Fig.5 element 530).
- With regard claim 19, Levy et al. further discloses wherein second logic further comprises impedance matching circuitry to match impedance of the second logic to the differential transmission line (column 7 lines 17-21 and column 8 lines 41-44).
- With regard claim 20, Levy et al. discloses an apparatus, comprising:

a device driver (Fig.6 element 600) to receive a multiphase encoded waveform (column 8 lines 38-50), having:

an amplifier (Fig.4 element 402) to receive differential signal levels (Fig.4 element 402 input, DIFF_DATA_INPUT and Fig.6 element 600 output, DIFF_DATA_OUT) representing the multiphase encoded waveform from a bus (Fig.2 element 206 and column 5 lines 2-58 and column 7 lines 11-21, where both driver (500 and 600) and receiver (400) are differential driver and receiver.) and extract the multiphase encoded waveform from the received differential signal levels (column 7 lines 40-51); and

a differential delayed lock loop (Fig.4 element 404) coupled to stretch a multiphase encoded waveform timing to a predetermined length (column 7 lines 44-51, where the third logic (Fig.4) of the Levys' reference is exactly the same (structure and connection and components) as that of the third logic (Fig.6) of the instant application, it is inherent that the differential DLL (404) of the Levys' third logic can perform the same function as that of the DLL (604) of the instant application, i.e. to stretch a multiphase encoded waveform timing to a predetermined length),

wherein the differential delay-lock loop includes logic to align rising edges of the received multiphase encoded waveform to rising edges of a transmitted multiphase encoded waveform (column 7 lines 40-51).

- With regard claim 21, Levy et al. further discloses wherein the third logic includes a register coupled to check data integrity of the multiphase encoded waveform (Fig.4 element DATA REGISTER AND INTEGRITY CHECK).
- With regard claim 22, Levy et al. further discloses wherein the register (Fig.4 element DATA REGISTER AND INTEGRITY CHECK) includes logic to extract data bits from the received multiphase encoded waveform (Fig.4 element 404 outputs) and to perform a probability analysis to determine a likelihood of errors.

Note that the Levy's reference teaches a DATA REGISTER AND INTEGRITY CHECK (logic) that appears to be the same as, or an obvious variant of, the DATA REGISTER AND INTEGRITY CHECK (logic) disclosed in the instant application. It is inherent that the Levy's DATA REGISTER AND INTEGRITY CHECK (logic) will perform the same function as that of the instant application. Under the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method (function) claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method (function), it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang